

Docket No. 244702US2

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

IN RE APPLICATION OF: Takeshi YOSHIDA, et al.

SERIAL NO: New Application

GAU:

FILED: Herewith

EXAMINER:

FOR: PROCESSING METHOD OF SEMICONDUCTOR SUBSTRATE

INFORMATION DISCLOSURE STATEMENT UNDER 37 CFR 1.97

COMMISSIONER FOR PATENTS
ALEXANDRIA, VIRGINIA 22313

SIR:

Applicant(s) wish to disclose the following information.

REFERENCES

- The applicant(s) wish to make of record the references listed on the attached form PTO-1449. Copies of the listed references are attached, where required, as are either statements of relevancy or any readily available English translations of pertinent portions of any non-English language references.
- A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

RELATED CASES

- Attached is a list of applicant's pending application(s) or issued patent(s) which may be related to the present application. A copy of the patent(s), together with a copy of the claims and drawings of the pending application(s) is attached along with PTO 1449.
- A check or credit card payment form is attached in the amount required under 37 CFR §1.17(p).

CERTIFICATION

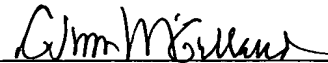
- Each item of information contained in this information disclosure statement was first cited in a communication from a foreign patent office in a counterpart foreign application not more than three months prior to the filing of this statement.
- No item of information contained in this information disclosure statement was cited in a communication from a foreign patent office in a counterpart foreign application or, to the knowledge of the undersigned, having made reasonable inquiry, was known to any individual designated in 37 CFR §1.56(c) more than three months prior to the filing of this statement.

DEPOSIT ACCOUNT

- Please charge any additional fees for the papers being filed herewith and for which no check or credit card payment is enclosed herewith, or credit any overpayment to deposit account number 15-0030. A duplicate copy of this sheet is enclosed.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.



Marvin J. Spivak

Registration No. 24,913

Customer Number

22850

Tel. (703) 413-3000
Fax. (703) 413-2220
(OSMMN 05/03)

C. Irvin McClelland
Registration Number 21,124

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STATEMENT OF RELEVANCY

Reference AO (2002-189000) of Form PTO-1449:

In this invention, in a semiconductor device with an integrated circuit formed on a semiconductor substrate surface, a hemispherical convex is integrated into the semiconductor substrate to be formed in a part of a rear surface of the semiconductor substrate. In this case, the hemispherical convex may constitute a part of the hemisphere. The hemispherical convex serves as a semiconductor solid immersion lens for performing rear surface analysis of the integrated circuit. The semiconductor substrate and the semiconductor solid immersion lens are integrated into each other.

When forming the semiconductor hemisphere on the semiconductor substrate rear surface, initially, a grinding tool 3 with a semicircular slot 3a in cross section is pressed against a semiconductor substrate rear surface 1b. Then, the grinding tool 3 is rotated with the normal passing through the center of the slot 3a as an axis while the semiconductor substrate is ground by an abrasive (not shown) (See Fig. 3(a)). As a result, a convex semiconductor hemisphere 1c is formed along the semicircular slot 3a with the rotation axis as the center (See Fig. 3(b)).

Form PTO 1449 (Modified)	U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY DOCKET NO. 244702US2	SERIAL NO. New Application			
LIST OF REFERENCES CITED BY APPLICANT		APPLICANT Takeshi YOSHIDA, et al.				
		FILING DATE Herewith	GROUP			
		U.S. PATENT DOCUMENTS				
EXAMINER INITIAL	DOCUMENT NUMBER	DATE	NAME	CLASS	SUB CLASS	FILING DATE IF APPROPRIATE
	AA					
	AB					
	AC					
	AD					
	AE					
	AF					
	AG					
	AH					
	AI					
	AJ					
	AK					
	AL					
	AM					
	AN					
FOREIGN PATENT DOCUMENTS						
	DOCUMENT NUMBER	DATE	COUNTRY	TRANSLATION		
				YES	NO	
	AO 2002-189000	07/05/02	Japan		X	
	AP					
	AQ					
	AR					
	AS					
	AT					
	AU					
	AV					
OTHER REFERENCES (Including Author, Title, Date, Pertinent Pages, etc.)						
	AW	Stephen B. IPPOLITO, et al., "HIGH-RESOLUTION IC INSPECTION TECHNIQUE", Department of Electrical and Computer Engineering and the Photonics Center, Boston University, (12 pages)				
	AX	Stephen B. IPPOLITO, et al., "COMPARISON OF NUMERICAL APERTURE INCREASING LENS AND STANDARD SUBSURFACE MICROSCOPY", Depts. of Physics and Electrical and Computer Engineering and the Photonics Center, Boston University, (2 pages)				
	AY	Stephen B. IPPOLITO, et al., "HIGH RESOLUTION SUBSURFACE MICROSCOPY TECHNIQUE", Boston University Photonics Center, Depts. of Physics and Electrical and Computer Engineering, (2 pages)				
	AZ					<input type="checkbox"/> Additional References sheet(s) attached
Examiner				Date Considered		
*Examiner: Initial if reference is considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.						